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TOWARD DESIGNING HIGH-SPEED COST-EFFICIENT QUANTUM REVERSIBLE CARRY SELECT ADDERS

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Abstract: Reversible logic efficiently prevents energy wastage through thermal dissipation. This project presents a comprehensive exploration introducing new carry-select adders (CSLA) based on quantum and reversible logic. Five reversible CSLA designs are proposed and compared, evaluating various criteria, including speed, quantum cost, and area, compared to previously published schemes. These comparative metrics are formulated for arbitrary n-bit size blocks. Each design type is described generically, capable of implementing carry-select adders of any size.

Keywords: Quantum Computing, Reversible Logic, Carry Select Adder, Quantum Gates.

Introduction: Reversible computing was started when the basis of thermodynamics of information processing was shown that conventional irreversible circuits unavoidably generate heat because of losses of information during the computation [1]. The different physical phenomena can be exploited to construct reversible circuits avoiding the energy losses. One of the most attractive architecture requirements is to build energy lossless small and fast quantum computers. Most of the gates used in digital design are not reversible for example NAND, OR and EXOR gates. A Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate. Each Reversible gate has a cost associated with it called Quantum cost. The Quantum cost of a Reversible gate is the number of 2*2 Reversible gates or Quantum logic gates required in designing. One of the most important features of a Reversible gate is its garbage output i.e., every input of the gate which is not used as input to other gate or as a primary output is called garbage output. In digital design energy loss is considered as an important performance parameter. Part of the energy dissipation is related to non-ideality of switches and materials. Higher levels of integration and new fabrication processes have dramatically reduced the heat loss over the last decades. The power dissipation in a circuit can be reduced by the use of Reversible logic. Landauer's [2] principle states that irreversible computations generates heat of K*Tln2 for every bit of information lost, where K is Boltzmann's constant and T the absolute temperature at which the computation performed. Bennett [3] showed that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design reversible circuit. Several such gates are proposed over the past decades. Arithmetic circuits such as Adders, Subtractors, Multipliers and Dividers are the essential blocks of a Computing system. Dedicated Adder/Subtractor circuits are required in a number of Digital Signal Processing applications. Several designs for binary Adders and Subtractors are investigated based on Reversible logic. Minimization of the number of Reversible gates, Quantum cost and garbage inputs/outputs are the focus of research in Reversible logic. The computers in the market are currently faster, smaller, and more complex than the previous ones. The cost for this speed and complexity

is higher power consumption. Therefore, power consumption in modern computers is a vital design issue. In this context, reversible circuits are of interest. These circuits perform only reversible operations, that is, they do not lose information during calculations, and therefore they can avoid power loss caused by information loss. In addition, in a computer system, most of the operations are based on sequential logic, as a result, sequential operations form an important part of the computing computer system. Many existing methods in the field of reversible sequential circuits mainly focus on the design of latches and reversible flip-flops [1–5]. The reversible design of sequential circuit components such as latches and flip-flops is shown in these articles and it is suggested that sequential circuits can be designed by replacing latches and flip-flops and other combinational gates in the irreversible current designs with their corresponding reversible components. Using this alternative method, researchers have proposed several designs for conventional sequential circuits such as counters and shift registers [1–16]. Even though many works have been done in the field of designing reversible sequential circuits using replacement technique, this replacement technique is not This article has been corrected with minor changes. These changes do not impact the academic content of the article. of much interest, because it leads to high quantum cost, fixed inputs, and garbage outputs. Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology.The heat generated due to the loss of one bit of

Reversible Gates: A digital combinational logic circuit is reversible if it maps each input pattern to a unique output pattern. There are many types of reversible gates including: inverter/NOT, Feynman, Toffoli, and Fredkin. Table 1 lists the behavior of each of these reversible gates.

Gate Type	Functionality
1*1 Not	$x^+ = \overline{x}$
2*2 Feynman [4]	$x^+ = x$ $y^+ = x \oplus y$
3*3 Toffoli [19]	$x^+ = x$ $y^+ = y$ $z^+ = xy \oplus z$
3*3 Fredkin [5]	$x^+ = x$ $y^+ = \overline{x}y \oplus xz$ $z^+ = \overline{x}z \oplus xy$

Table 1: Gate functionality

EXISTING METHOD:

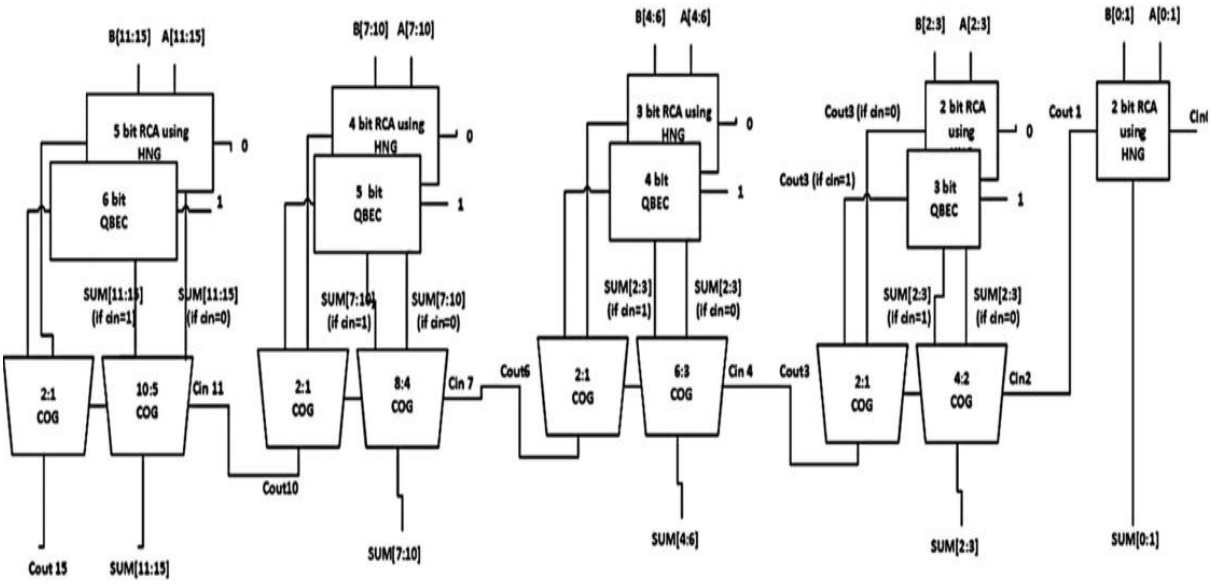


Figure.1 16-bit reversible QBEC square root CSLA with variable adder block size

The 16-bit reversible RCA square root CSLA presented is modified using the new proposed QBEC modules. In different stages, the m-bit RCA modules with Cin = 1 input signal are replaced by (m+1)-bit QBEC circuits (above figure). The effect of applying these new proposed modules in quantum cost and delay of the carry select adder structure is analyzed as follows: The total quantum cost of the proposed design is calculated by summating the quantum cost of 2, 2, 3, 4, and 5-bit RCA blocks, 2:1 multiplexers, and 3, 4, 5, and 6-bit QBEC modules used in the structure equal to 222. In a general manner for n-bit design, the total quantum cost of the proposed method is determined by (5), assuming that HNG, COG, and the proposed QBEC modules are applied in the structure as they are optimized in terms of quantum cost:

$$QC = 10(n-S) + 6S + 4K + \sum_{S}^{L} (block\ size)^2$$

The term written in the form of sigma summation calculates the total quantum cost of all QBEC modules, and the rest of the formula computes the total quantum cost of RCA circuits and multiplexer modules. This calculation has been formalized based on the overall size of the adder structure (n), the size of the smallest block (S), the total size of all blocks except the smallest one (n-S), and the number of stages (K). The delay of the new proposed approach depends on the size of the structure's largest stage, exactly like the method proposed in Section III.4. Providing that L denotes the largest stage's size, this stage requires an L-bit RCA module, which propagates the Cout signal with a delay equal to 6L. Then, the RCA module's output values enter an (L+1)-bit QBEC circuit having a propagation delay equal to L2. Next, the QBEC module generates a Cout signal assuming Cin = 1. However, the RCA circuit calculates the value of this signal when Cin = 0. Afterward, a 2:1 multiplexer with a delay of 4 selects between the two Cout signals resulted from the RCA and QBEC modules. As a result, the total delay of the proposed method is calculated by the following formula where L refers to the largest block size, which is at least one bit larger than its previous stages: L2+ 6L+4.

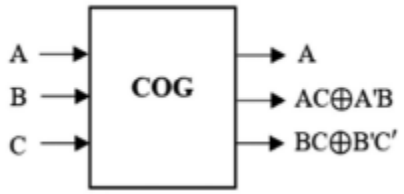


Fig:2 COG Gate,

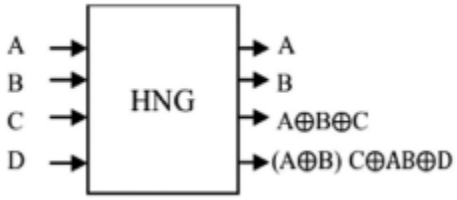
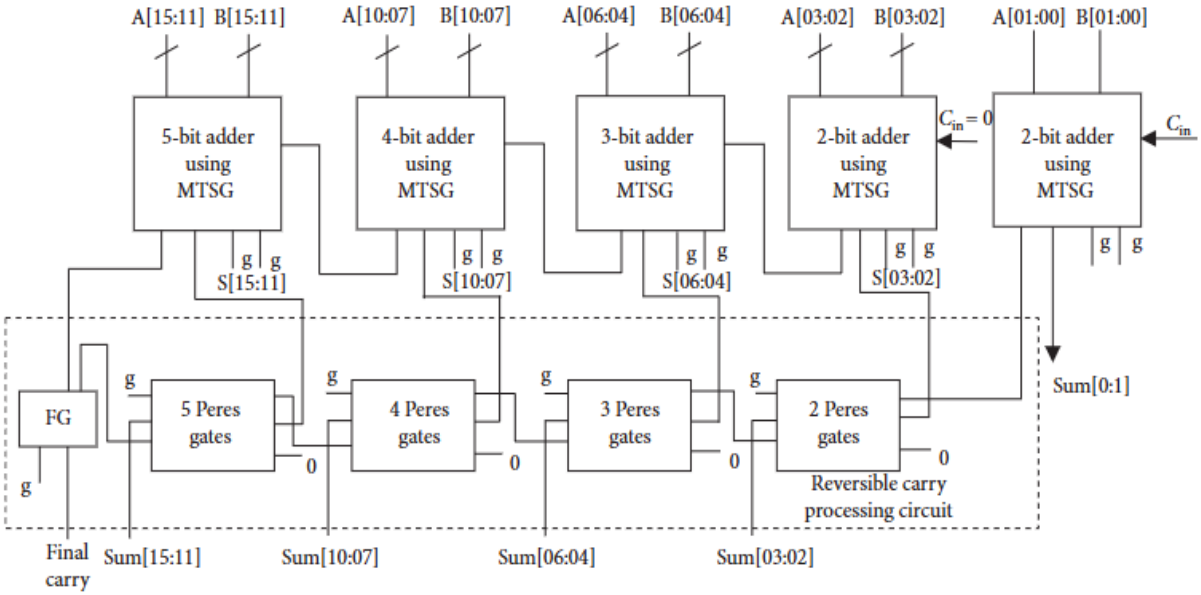


Fig:3 HNG Gate.

HNG and COG gates are chosen to be used as adders and multiplexers in this design, respectively, since they have minimum possible quantum cost and delay among their functionally similar reversible gates. The quantum cost and delay of the HNG gate are equal to 6 and 6; for the COG gate, these criteria are equal to 4 and 4, respectively. Designing an n-bit CSLA circuit based on the proposed approach needs (2n-1) bit full adder units and (2n-2) number of multiplexers provided that parallel addition executes through single-bit full adder modules. Therefore, the proposed circuit's quantum cost (considering HNG and COG gate as full adder and multiplexer) equals 20n-14 in the n-bit scale.

PROPOSED METHOD:

EFFICIENT DESIGN FOR A REVERSIBLE CARRY SELECT ADDER (ERCSA)



F IGURE4: 16-bit ERCSA

PG Gates: Each single-bit adder is paired with a PGgate to handle carry propagation effectively.• FG Gate: Positioned at the end of the 5-bit adder, theFG gate computes the final carry output (Cout).The reversible nature of these gates ensures energy-efficient operation while maintaining the integrity of the computational process. The architecture of 16-bit ERCSA is shown in Figure. The above circuit is considered reversible because:1. All components (MTSG, Peres gates) are individually reversible (bijective mappings).2. The carry propagation uses reversible logic (Peres gate chain), not MUXs.3. The number of inputs = outputs, preserving information.4. There is no fan-out, feedback, or data loss, ensuring Landauer's condition is met. Although Feynman gates are often used for duplication in reversible logic, in this architecture they are not employed for fanout. Instead, the Feynman gate is integrated into the reversible carry processing circuit, where it assists in adjusting the sum and carry outputs in conjunction with Peres gates.

RESULTS:

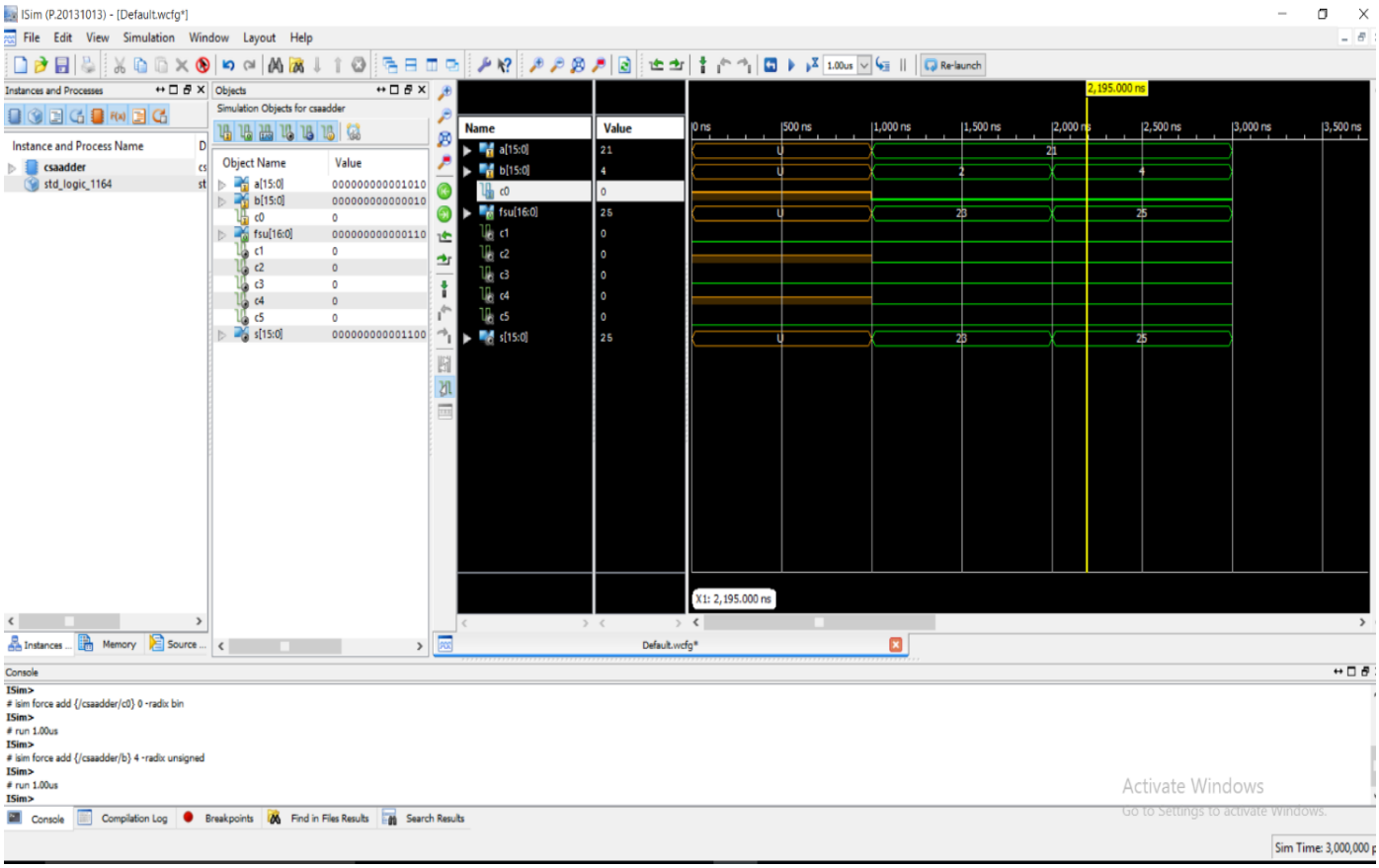


Fig:a Proposed Simulation results

The proposed 16-bit adder using a Modified Carry Select Adder (MCSA) with Reversible Quantum Logic was designed and simulated to evaluate its performance in terms of delay, area, and power consumption. The design was implemented using HDL (Verilog/VHDL) and verified through simulation tools such as Vivado and synthesied. The simulation results confirm that the proposed 16-bit adder performs correct arithmetic operations for all possible input combinations. The waveform analysis shows accurate sum and carry outputs corresponding to given input operands, validating the logical correctness of the design. The integration of reversible logic gates (such as Peres and Toffoli gates) ensures that the computation is lossless, preserving input information and reducing unnecessary bit transitions.

ADVANTAGES:

They are easy to design as it reduces the amount of wiring and occupy less space.

They are helpful in tracking the information (data).

Delaying a signal is easy with low power consumption

Less combinational path delay

Low area over head

APPLICATIONS:

The applications include:

They are implemented in devices like computers and calculators as they serve as temporary data storage spaces.

They were used to handle data processing in the former years of Computer Technology..

They are used to add more binary inputs to a Microprocessor as it has fixed number of I/O pins.

They are also used as Delay Circuits.

They are used as Sequence Generator and Counters.

CONCLUSION:

Finally, this project proposes and implements a new CSLA circuits in reversible logic. This study aims to achieve a very high-speed optimization in the addition operation. To do so, we proposed a reversible and quantum adder structure that can balance the trade-off between different criteria and increasing speed. Furthermore, a reversible quantum binary to excess one circuit has been proposed, ultimately a novel structure in reversible logic. The delay and quantum cost of all five proposed approaches are formalized, compared to each other and their existing counterparts. Comparative results show that the optimized scheme for designing a cost and delay-efficient reversible and quantum CSLA structure is multi-bit variable-sized carry select addition stages, which can realize the combination of RCA blocks and square root approach. The proposed high-speed quantum reversible adder structure can develop large-scale nanotechnology and massive qubit computational quantum systems.

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